



Japan's STARC Adopts Extreme GoldTime as Timing Tool in STARCAD-CEL (V4.0) Statistical IC Analysis Flow

Advanced Multi-Mode/Multi-Corner Analysis and Runtime Performance Are Key Reasons

Santa Clara, Calif., June 9, 2010 — Extreme DA™ announced that Japan's leading semiconductor research organization, the Semiconductor Technology Academic Research Center (STARC), has confirmed the Extreme DA GoldTime™ timing analyzer is being used for STARC's statistical static timing analysis (SSTA) flow in STARCAD-CEL (V4.0). STARC has preliminarily released this flow to its member companies. GoldTime was first chosen by STARC in 2007 and has been part of STARCAD-CEL since that date.

Variation Analysis Software Required for IC Designs at 45-nm and Below

At advanced semiconductor process nodes of 45-nm and below, software is required for analyzing environmental, systematic and random variations that affect the performance of IC designs. Variation-aware analysis helps designers understand what these effects have on achieving timing targets for their IC designs.

The Multi-Mode / Multi-Corner (MMMC) features of GoldTime have been evaluated in the STARCAD-CEL (V4.0) environment. Because of GoldTime's multi-threaded runtime speed, IC designers can quickly investigate how extremes in the electrical environment, combined with different IC operating modes and variations in semiconductor manufacturing process will affect the final performance and yield of the design in production.

"Our member companies have available to them an advanced, timing sign-off solution that provides the necessary analysis for digital designs," said Nobuyuki Nishiguchi, vice-president and general manager of Development Department-1 at STARC. "The STARCAD-CEL (V4.0) flow using statistical and multi-mode / multi-corner technology in Extreme DA GoldTime delivers excellent runtimes that can match the performance of traditional static timing tools for appropriate number of corners. STARC members will see reductions in turn-around-time, and looser design margins in near future."

"The continuing use by STARC of Extreme DA GoldTime in the statistical STARCAD-CEL flow is a strong endorsement of the technological leadership of our timing solution," said Mustafa Celik, president and CEO of Extreme DA. "The speed, accuracy, and capabilities of

our analysis continue to advance. Our collaboration with STARC will lead to new kinds of analysis that will be crucial for makers of advanced IC designs.”

The Semiconductor Technology Academic Research Center, STARC, is a research consortium co-founded by major Japanese semiconductor companies in December 1995. STARC's mission is to contribute to the growth of the Japanese semiconductor industry by developing leading-edge SoC design technologies.

About Extreme DA

Headquartered in Santa Clara, Calif., venture-funded Extreme DA develops and licenses software products for the timing sign-off of integrated circuits at 65-nanometer and below. The company's investors include Foundation Capital, IT-Farm Corporation, and Lanza techVentures. For the latest news and information on Extreme DA, visit www.extreme-da.com or write to info@extreme-da.com.

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